

What is claimed is:

1. A circuit comprising:
 - a shift register, comprising an input port, to provide a set of output voltages representative of a set of Boolean values;
 - a set-reset flip-flop, comprising an input port, to provide at the input port of the shift register a voltage representative of an output Boolean value of the set-reset flip-flop;
 - and
 - logic to provide at the input port of the set-reset flip-flop a voltage representative of the Boolean AND of a subset of the set of Boolean values of the shift register.
2. The circuit as set forth in claim 1,
 - wherein the set-reset flip-flop comprises an S input port and a R input port, where the input port of the set-reset flip-flop is the R input port.
3. A circuit comprising:
 - a shift register having a state of N-1 Boolean values $Q\langle i \rangle$, $i = 1, 2, \dots, N-1$, wherein in response to a clock signal the state changes so that $Q\langle i-1 \rangle$ is shifted into $Q\langle i \rangle$ for $i = 2, \dots, N-1$;
 - a set-reset flip-flop comprising a SET input port having a voltage to represent a Boolean value S and a RESET input port having a voltage to represent a Boolean value R, the set-reset flip-flop to provide an output voltage representative of a Boolean value $Q\langle 0 \rangle$, wherein in response to the clock signal $Q\langle 0 \rangle$ is a Boolean 1 when S is a Boolean 1 and $Q\langle 0 \rangle$ is a Boolean 0 when R is a Boolean 1, and wherein $Q\langle 0 \rangle$ does not change in response to the clock signal when both S and R are a Boolean 0, wherein in response to the clock signal $Q\langle 0 \rangle$ is shifted into $Q\langle 1 \rangle$; and
 - logic to provide at the RESET input port a voltage representative of the Boolean value $\{Q\langle L-1 \rangle \wedge Q\langle L-2 \rangle \wedge \dots \wedge Q\langle 0 \rangle\}$ where $\wedge$ is a Boolean AND and L is a positive integer not greater than N.

4. The circuit as set forth in claim 3, wherein the logic is to further provide at the SET input port a voltage representative of the Boolean value $\{Q^{#<M-1>} \wedge Q^{#<M-2>} \wedge \dots \wedge Q^{#<0>}\}$ where $Q^{#<i>}$ is the Boolean complement of $Q^{<i>}$ and M is a positive integer not greater than N.

5. A circuit comprising:
 - a shift register having a state of N-1 Boolean values $Q^{<i>}$, $i = 1, 2, \dots, N-1$, wherein in response to a clock signal the state changes so that $Q^{<i-1>}$ is shifted into $Q^{<i>}$ for $i = 2, \dots, N-1$;
 - a set-reset flip-flop comprising a SET input port having a voltage to represent a Boolean value S and a RESET input port having a voltage to represent a Boolean value R, the set-reset flip-flop to provide an output voltage representative of a Boolean value $Q^{<0>}$, wherein in response to the clock signal $Q^{<0>}$ is a Boolean 1 when S is a Boolean 1 and $Q^{<0>}$ is a Boolean 0 when R is a Boolean 1, and wherein $Q^{<0>}$ does not change in response to the clock signal when both S and R are a Boolean 0, wherein in response to the clock signal $Q^{<0>}$ is shifted into $Q^{<1>}$; and
 - logic to provide at the SET input port a voltage representative of the Boolean value $\{Q^{#<M-1>} \wedge Q^{#<M-2>} \wedge \dots \wedge Q^{#<0>}\}$, where $\wedge$ is a Boolean AND, $Q^{#<i>}$ is the Boolean complement of $Q^{<i>}$, and M is a positive integer not greater than N.

6. A system comprising:
 - a clock circuit to provide a clock signal, the clock signal having a first transition and a second transition in each clock cycle;
 - a shift register having a state of N-1 Boolean values $Q^{<i>}$, $i = 1, 2, \dots, N-1$, wherein on each of the first transitions of the clock signal the state changes so that $Q^{<i-1>}$ is shifted into $Q^{<i>}$ for $i = 2, \dots, N-1$;
 - a set-reset flip-flop comprising a SET input port, a RESET input port, a clock input port to receive the clock signal, and to provide an output voltage representative of a Boolean value $Q^{<0>}$ on each of the first transitions of the clock signal so that $Q^{<0>}$ is shifted into $Q^{<1>}$; and

logic to provide at the RESET input port a voltage representative of the Boolean value $\{Q_{<L-1>} \wedge Q_{<L-2>} \wedge \dots \wedge Q_{<0>}\}$ where $\wedge$ is a Boolean AND and L is a positive integer not greater than N.

7. The system as set forth in claim 6, the logic to further provide at the SET input port a voltage representative of the Boolean value $\{Q_{<M-1>}^{\#} \wedge Q_{<M-2>}^{\#} \wedge \dots \wedge Q_{<0>}^{\#}\}$ where $Q_{<i>}^{\#}$ is the Boolean complement of $Q_{<i>}$ and M is a positive integer not greater than N.

8. The system as set forth in claim 6, wherein the first transition is a rising transition.

9. The system as set forth in claim 6, wherein the first transition is a falling transition.

10. A system comprising:

a clock circuit to provide a clock signal, the clock signal having a first transition and a second transition in each clock cycle;

a shift register having a state of N-1 Boolean values $Q_{<i>}$, $i = 1, 2, \dots, N-1$, wherein on each of the first transitions of the clock signal the state changes so that $Q_{<i-1>}$ is shifted into $Q_{<i>}$ for $i = 2, \dots, N-1$;

a set-reset flip-flop comprising a SET input port, a RESET input port, a clock input port to receive the clock signal, and to provide an output voltage representative of a Boolean value $Q_{<0>}$ on each of the first transitions of the clock signal so that $Q_{<0>}$ is shifted into $Q_{<1>}$; and

logic to further provide at the SET input port a voltage representative of the Boolean value $\{Q_{<M-1>}^{\#} \wedge Q_{<M-2>}^{\#} \wedge \dots \wedge Q_{<0>}^{\#}\}$, where $\wedge$ is a Boolean AND, $Q_{<i>}^{\#}$ is the Boolean complement of $Q_{<i>}$, and M is a positive integer not greater than N.

11. The system as set forth in claim 10, wherein the first transition is a rising transition.

12. The system as set forth in claim 10, wherein the first transition is a falling transition.

13. A circuit to divide down the frequency of an input clock signal, the circuit comprising:

a shift register;

a set-reset flip-flop comprising a set input port, a reset input port, and an output port coupled to the shift register; and

combinational logic to provide feedback from the shift register and the set-reset flip-flop to at least one of the set or reset input ports.